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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/316,699	05/21/1999	WILLIAM J. DALLY	AVI99-01	8189

21005 7590 11/20/2002

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EXAMINER

LY, ANH VU H

ART UNIT

PAPER NUMBER

2662

DATE MAILED: 11/20/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

17G

Office Action Summary	Application No.	Applicant(s)	
	09/316,699	DALLY ET AL.	
	Examiner	Art Unit	
	Anh-Vu H Ly	2662	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on amendment filed on 08/29/2002.
- 2a) This action is **FINAL**. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-49 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-10, 13-25 and 28-49 is/are rejected.
- 7) Claim(s) 11, 12, 26 and 27 is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) The proposed drawing correction filed on 29 August 2002 is: a) approved b) disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
 - a) The translation of the foreign language provisional application has been received.
- 15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

<ol style="list-style-type: none"> 1)<input checked="" type="checkbox"/> Notice of References Cited (PTO-892) 2)<input checked="" type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) 3)<input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) <u>8</u>. 	<ol style="list-style-type: none"> 4)<input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____. 5)<input type="checkbox"/> Notice of Informal Patent Application (PTO-152) 6)<input type="checkbox"/> Other: _____.
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DETAILED ACTION

Response to Amendment

1. This communication is in response to applicant's amendment filed on August 29, 2002. The proposed amendment to the claims has been entered. Claims 1-49 are pending.

Drawings

2. Figure 4 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g).

Claim Objections

3. Claim 29 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

4. Claims 1-7, 13-22, 28-35, 38-43, and 45-49 are rejected under 35 U.S.C. 102(a) as being anticipated by Ben-Michael et al (EP O 886 454 A2). Hereinafter, referred to as Ben-Michael.

With respect to claims 1-3, 5-7, 13-15, 31-33, 35, 38-41, 43, 45-47, and 49, Ben-Michael discloses (page 5, line 20 – page 6, line 33; page 7, line 41-42 and Fig. 7) a block diagram illustrating on-chip memory and off-chip memory for storing data packets or credits; Wherein, on-chip memory allows rapid access for reading and writing (a first set of rapidly accessible buffers which store information units received at an input link) and wherein, off-chip memory involves a delay in accessing and processing data packets or credits (a second set of buffers for the information units that are accessed more slowly than the first set).

With respect to claims 4, 19, 34, 42, Ben-Michael discloses on page 5, line 41-43 that the chip memory is a SRAM (a buffer pool) wherein SRAM is divided into four consecutive parts to form the logical banks. Ben-Michael disclose on page 6, line 1-2, there is a pointer which points to the part of the SRAM from which credits are being read (a pointer array of pointers to buffered information units).

With respect to claims 16-18, 20-22, 28-30, and 48, Ben-Michael discloses (page 5, line 20 – page 6, line 33; page 7, line 41-42 and Fig. 7) a block diagram illustrating on-chip memory and off-chip memory for storing data packets or credits; Wherein, on-

chip memory allows rapid access for reading and writing (storing information units received at an input link in a first set of rapidly accessible buffers) and wherein, off-chip memory involves a delay in accessing and processing credits or data. The off-chip memory is accessed only when the on-chip memory is full (storing overflow from first set of buffers in second set of buffers that are accessed more slowly than first set).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 8-10, 23-25, 36-37, and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ben-Michael.

With respect to claims 8-10, 23-25, 36-37, and 44, Ben-Michael discloses a method and apparatus for storing data packets or credits in an ATM network in on-chip memory and off-chip memory. Ben-Michael does not disclose a flow control to stop the arrival of new information units while transferring information units between the first set of buffers and the second set of buffers. However, such flow control for stopping the arrival of new information units is well known in the art and has been applied in many applications such as credit-based flow control, rate-based flow control, etc.... Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to include a credit-based or rate-based flow control in Ben-

Michael's system, for controlling data transmission between the nodes in order to prevent an overflow in the network.

Allowable Subject Matter

6. Claims 11-12 and 26-27 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

7. Applicant's arguments with respect to claims 1-45 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Joo, Y. M. et al "Doubling Memory Bandwidth for Network Buffers" INFOCOM '98, Seventeenth Annual Joint Conference of the IEEE Computer and Communications Societies, Vol. 2, 29 March – 2 April 1998, pages 808-815.

Rhee, Yunseok et al "A Scalable Cache Coherent Scheme Exploiting Wormhole Routing Networks" High-Performance Computer Architecture, 9-13 Jan. 1999, pages 223-226.

Besson, E. "Performance Evaluation of Hierarchical Caching in High-Speed Routers" Global Telecommunications Conference, Vol. 5, 8-12 Nov. 1998, pages 2640-2645.

Daniel et al (US Patent No. 6,373,846) discloses a single chip networking device with enhanced memory accessed co-processor.

Hauser et al (US Patent No. 6,115,748) discloses a prioritized access to shared buffers.

Venkataraman (US Patent No. 5,802,052) discloses a scalable high performance switch element for a shared memory packet or ATM cells switch fabric.

Manning et al (US Patent No. 6,256,674) discloses a method and apparatus for providing buffers state flow control at the link level in addition to flow control on a per-connection basis.

Yasue et al (US Patent No. 6,189,03) discloses a communication control system utilizing a shared buffer managed by high and low level protocols.

Pal et al (US Patent No. 6,272,567) discloses a system for interposing a multiport internally cached DRAM in a control path for temporarily storing multicast start of packet data until such can be passed.

Muller et al (US Patent No. 6,021,132) discloses a shared memory management in a switched network element.

Thorson (US Patent No. 6,055,618) discloses a virtual maintenance network in multiprocessing system having a non-flow controlled virtual maintenance channel.

Kadambi et al (US Patent No. 6,335,932) discloses a high performance self-balancing low cost network switching architecture based on distributed hierarchical shared memory.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh-Vu H Ly whose telephone number is 703-306-5675. The examiner can normally be reached on Monday-Friday 7:00am - 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hassan Kizou can be reached on 703-305-4744. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9314 for regular communications and 703-872-9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-4750.

av
November 7, 2002



HASSAN KIZOU
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600